



Dokumentacja projektu moduły zabezpieczających przed przepięciami OVP dla detektora mozaikowego PDX dla eksperymentu BelleII.

1. Wstęp
2. Projekt
3. Produkcja
4. Testy

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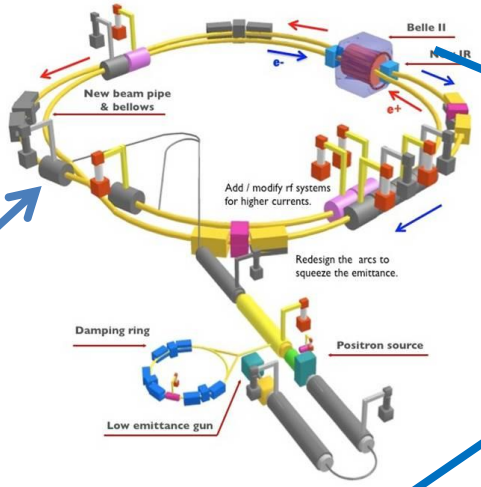
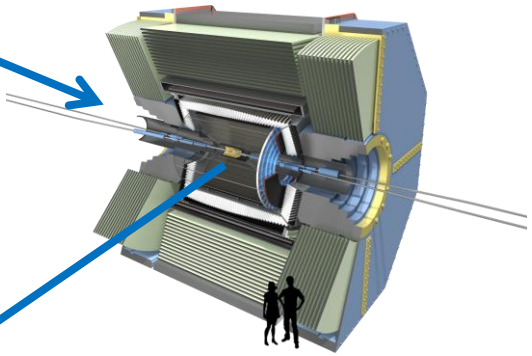
SuperKEKB

Belle II

KEK [HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION]

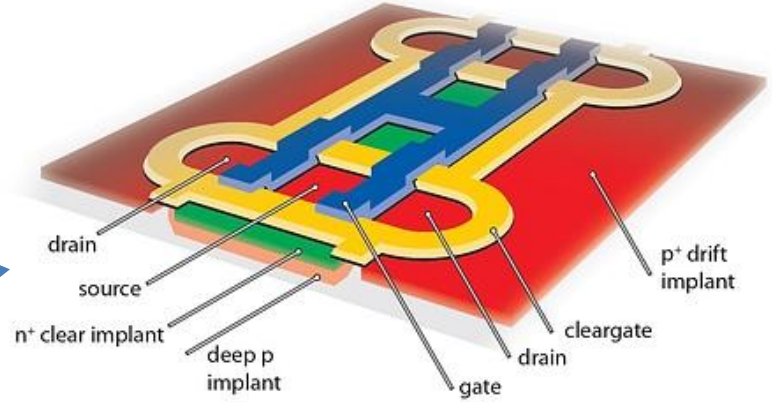








PXD detector



DEPFET – Depleted P-channel Field Effect Transistor

Umiejscowienie detektora PXD w eksperymencie BelleII.

Wstęp

- Przedstawiono historię technologii DEPFET, na której oparto projekt półprzewodnikowego mozaikowego detektora PXD.

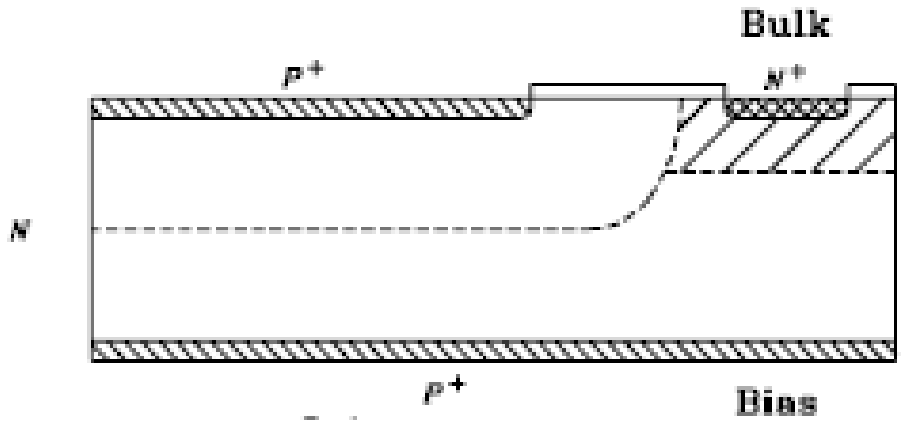
Gatti, E.; Rehak, P. Semiconductor drift chamber—An application of a novel charge transport scheme. *Nucl. Instrum. Methods Phys. Res. Sect. A* **1984**, *225*, 608–621. [CrossRef]

Emilio Gatti (1922 – 2016) Politechnika w Mediolanie

Pavel Rehak (1945 – 2009), Praga,Pisa, Karlsruhe, CERN, BNL (Brookhaven)

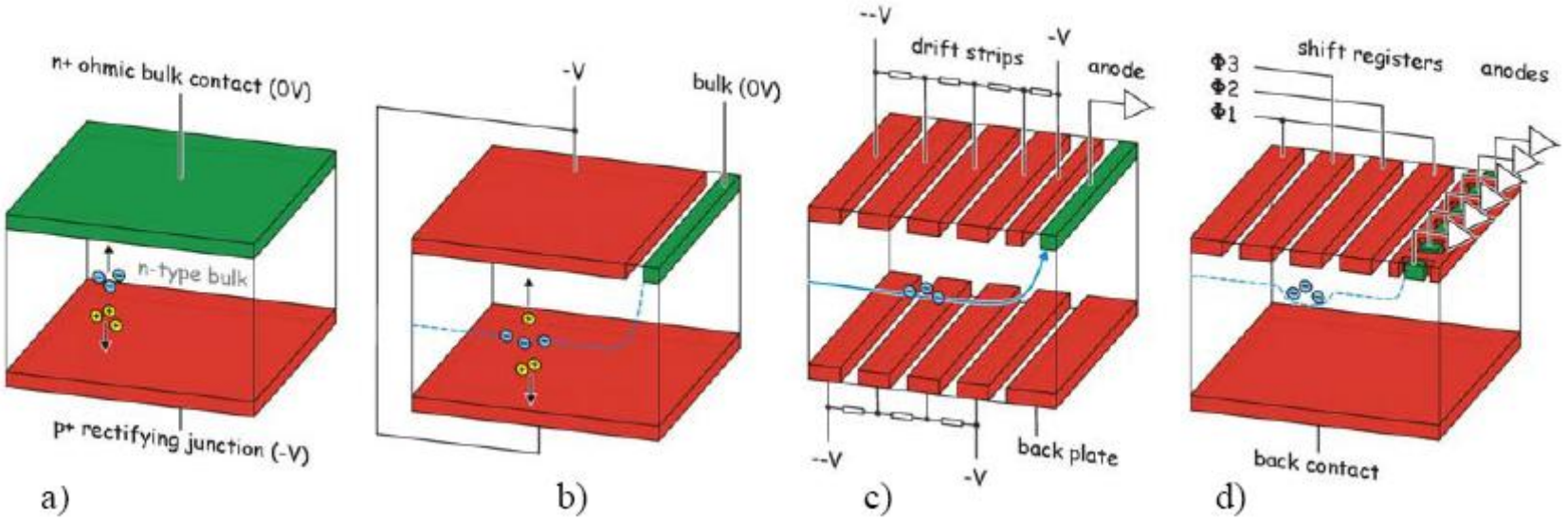
https://www.bnl.gov/pavelrehak/

W październiku 1983 roku, w ciągu miesiąca bardzo intensywnej pracy, Pavel Rehak i Emilio Gatti wpadli na pomysł półprzewodnikowego detektora dryfowego. Ich pomysł nie był zgodny z konwencjonalnym myśleniem w tym czasie.
Ich propozycja polegała na tym, że cienki płatek krzemu (n.p. typu n z domieszkowaniem p+ po dwóch stronach) może być zubożony o wolne nośniki (elektrony w tym przypadku) z małego kontaktu n+ (anoda o średnicy 100 um)



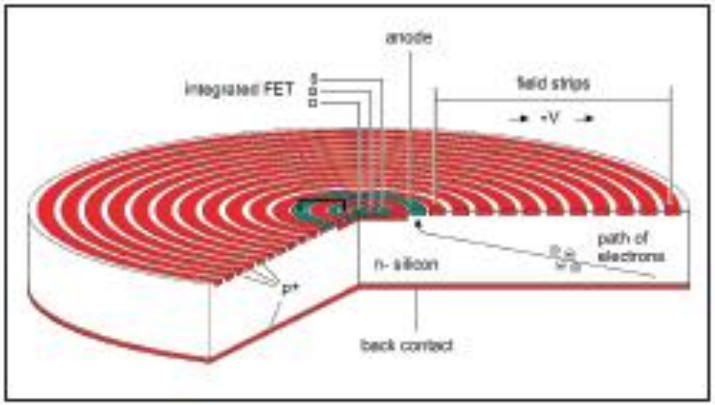


Basic semicoductor detector structures

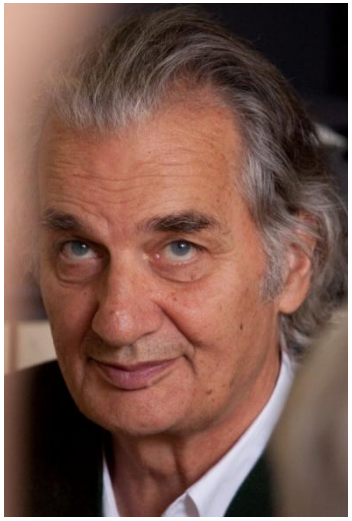


a) Reverse biased diode
b) Sideward depletion structure, basis of semoconductor drift detector
c) Drift detector
d) Pn - CCD

Elektrony wytwarzane przez cząstkę jonizującą mogą dryfować wzdłuż detektora przez zastosowanie pola elektrycznego.



Kemmer, J.; Lutz, G. New semiconductor detector concepts. *Nucl. Instr. Meth. A* **1987**, *253*, 365–377. [CrossRef]



Gerhard Lutz (1939 – 2017) był współzałożycielem :
Max-Planck-Institute Halbleiterlabor (1990)
http://www.hll.mpg.de

PNSensor (2002)
http://www.pnsensor.de/Willkommen/index.php

PNDetector (2007)
http://pndetector.de



Jozef Kemmer (1989 - 2007)

założył rodzinne przedsiębiorstwo KETEK GmbH w Monachium.

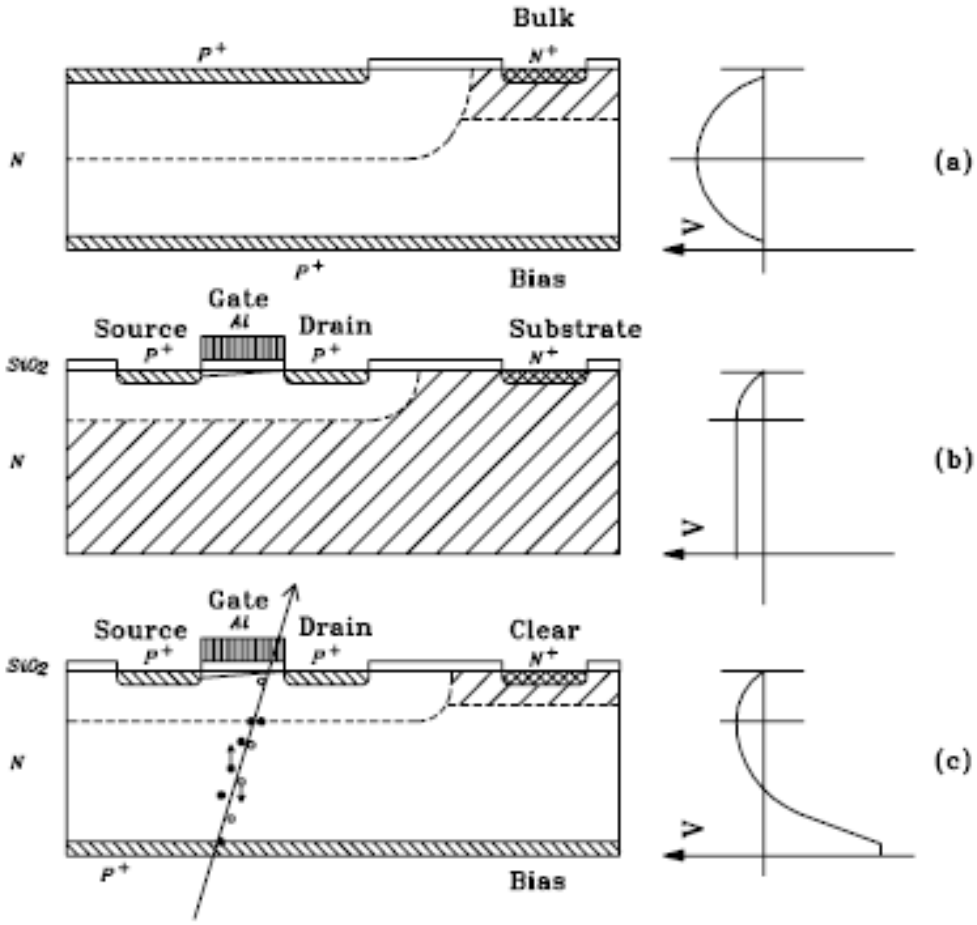
https://www.ketek.net/

KETEK is the world's leading manufacturer of Silicon Drift Detectors

Gerhard Lutz, Semiconductor Radiation Detectors, Springer-Verlag Berlin Heidelberg 1999,2007

DEPFET = SIDEWAY DEPLETION + FIELD EFFECT TRANSISTOR

(c) = (a) + (b)



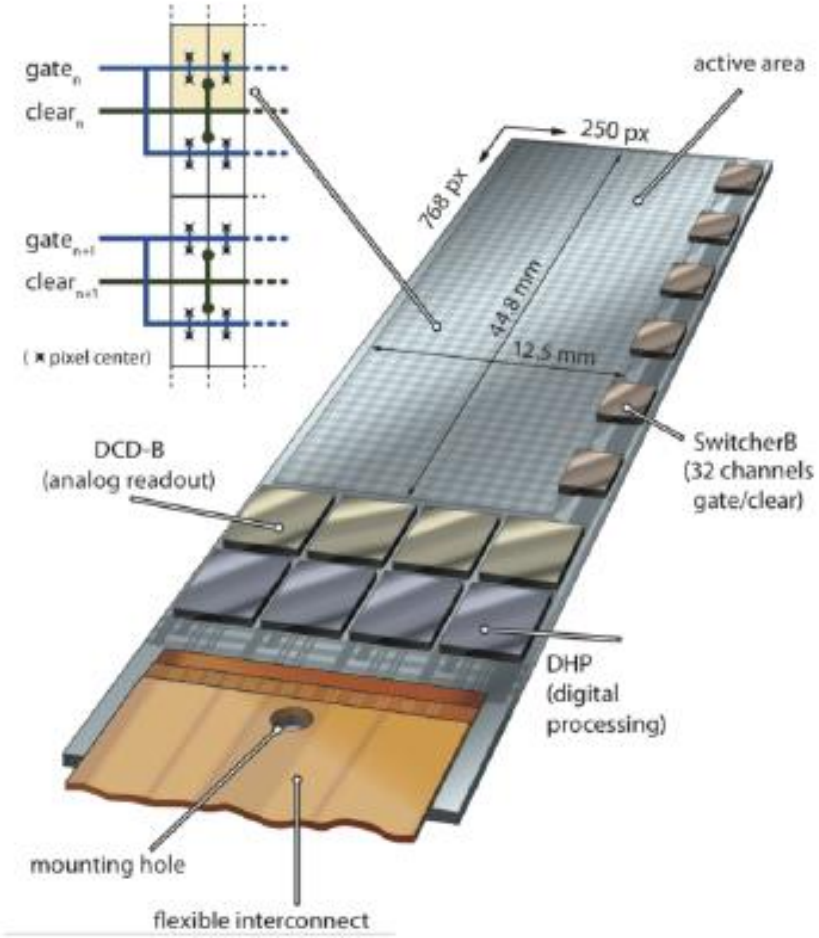
SIDEWAY DEPLETION METHOD

Field Effect Transistor structure

DEPFET

Fig. 9.4a–c. Concept of DEPFET detector–amplification structure (c) developed by combining the sideways depletion method (a) with the field effect transistor structure (b)

The proposed two layer vertex detector consists of 'all-silicon' modules: The read-out and control ASICs will be bump bonded on the rigid edges of the DEPFET substrate whereas in the region of the active pixel matrix the substrate will be thinned down to 75 µm. The front-end electronics is subdivided in three different ASIC types: One chip will provide up to 20 V output swing for the control voltages of the DEPFET matrix (SWITCHER), the current signals are being digitized by a multichannel ADC chip (DCD) and the processing of the digital data and module control functionality is implemented in a data handling chip (DHP) described below.



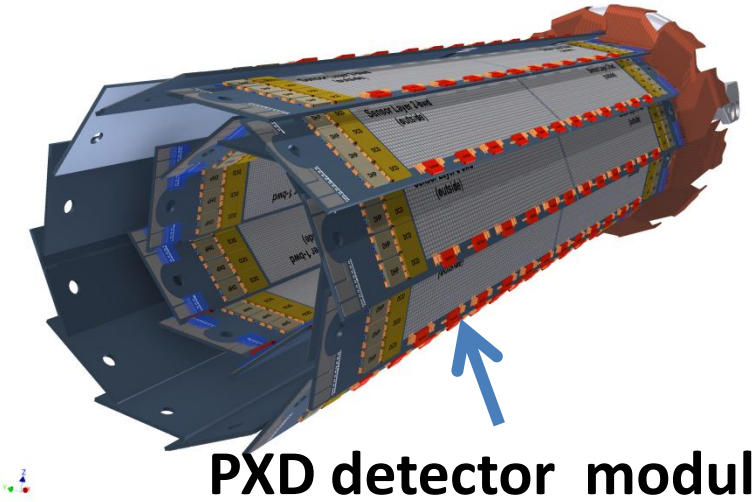
Opis modułu PXD

Power Supply for the DEPFET sensors and the readout ASICs per one module.

PXD detector: two layers, inner (8 modules x 2), outer (12 modules x 2), 40 modules in total.

Short name	V [V]nominal/range	I [mA]max	Comment
DHP_IO	+1.8/+1.6 to +2	160	
SW_DVDD	+1.8	24	
DHP_CORE	+ 1.2/+1.0 to +1.3	580	
DCD_DVDD	+ 1.8/+1.6 to +2	1000	
Digital Ground			
DCD_REFIN	+ 1.1/+0.9 to +1.4	360	
VSource	0 to +7	100	
AmpLow	+ 0.35	-1000	current sink
DCD_AVDD	+1.8/+1.6 to +2	2300	
Analog Ground			
GATE_ON1	-13 to -3	60	
GATE_ON2	-13 to -3	60	
GATE_ON1	-13 to -3	60	
GATE_OFF	-3 to +5	60	
CCG1	-10 to +1	10	
CCG2	-10 to +1	10	
CCG3	-10 to +1	10	
VDrift	-12 to -5	10	
Gate Ground			
Clear_High	+7 to +25	60	
Clear_Low	0 to +5	60	
SW_RefIn	SW_SUB + 3.3V	0.6	negative
SW_SUB	< -13	0.6	lowest of all
High Voltage	- 80		depletion
VGuard	-7 to 0		
BULK	+5 to +15	10	
Steering Ground			



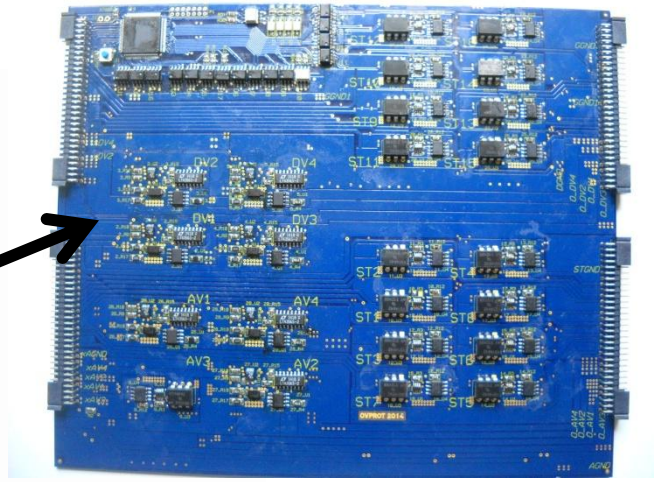


PXD detector module

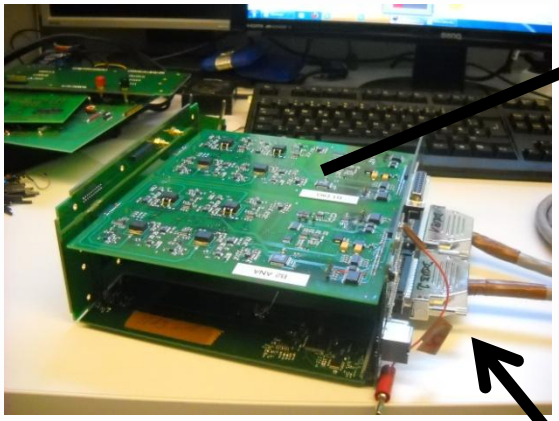
Detektor PXD i lista napięc zasilających jeden moduł.

Power Supply System of the PXD detector (one segment of 40)

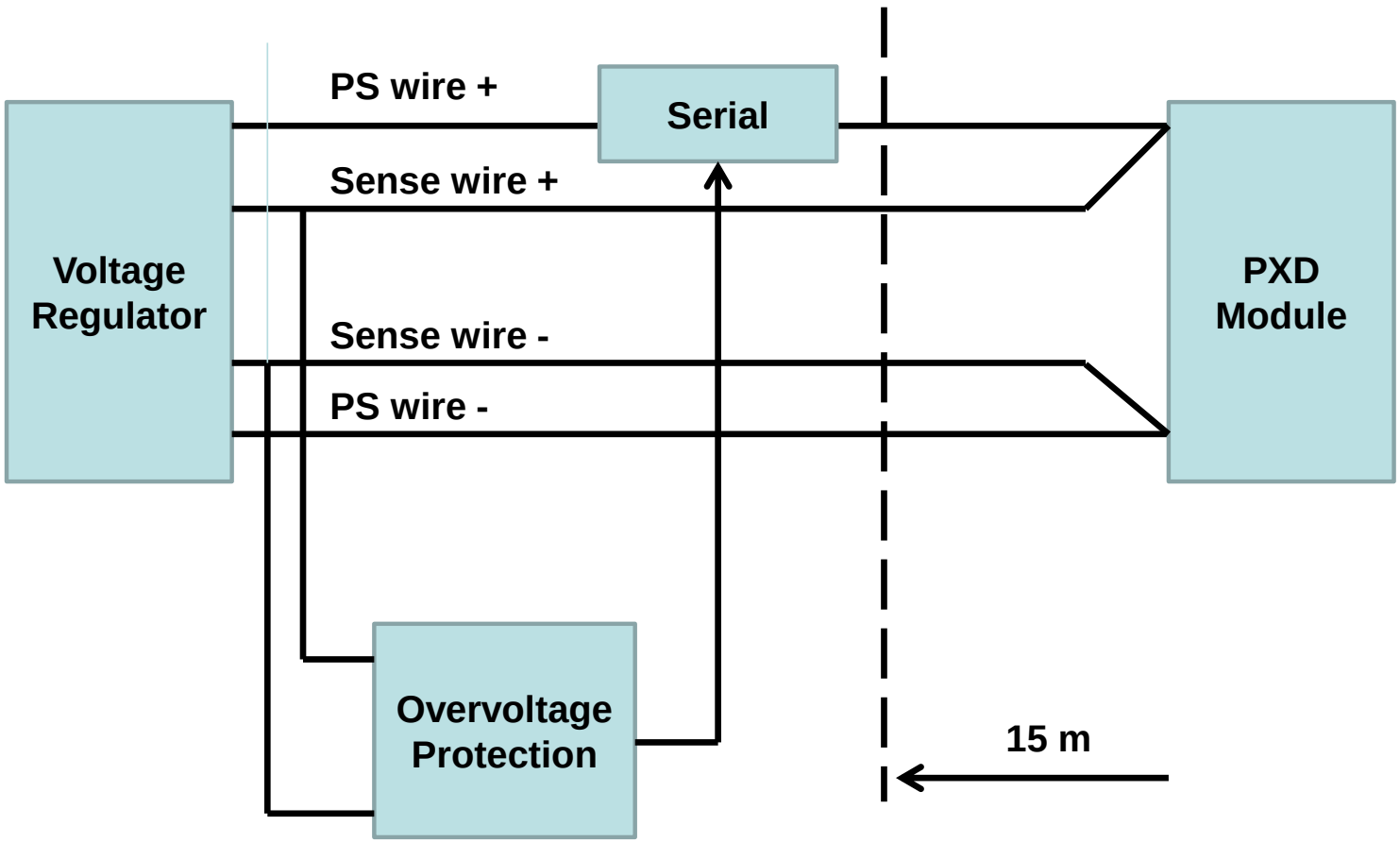
Overvoltage Protection module (OVP)



Power Supply module 40 modules in total



Schemat zasilania modułu PXD



Zasada protekcji jednego kanału.

System zabezpieczeń

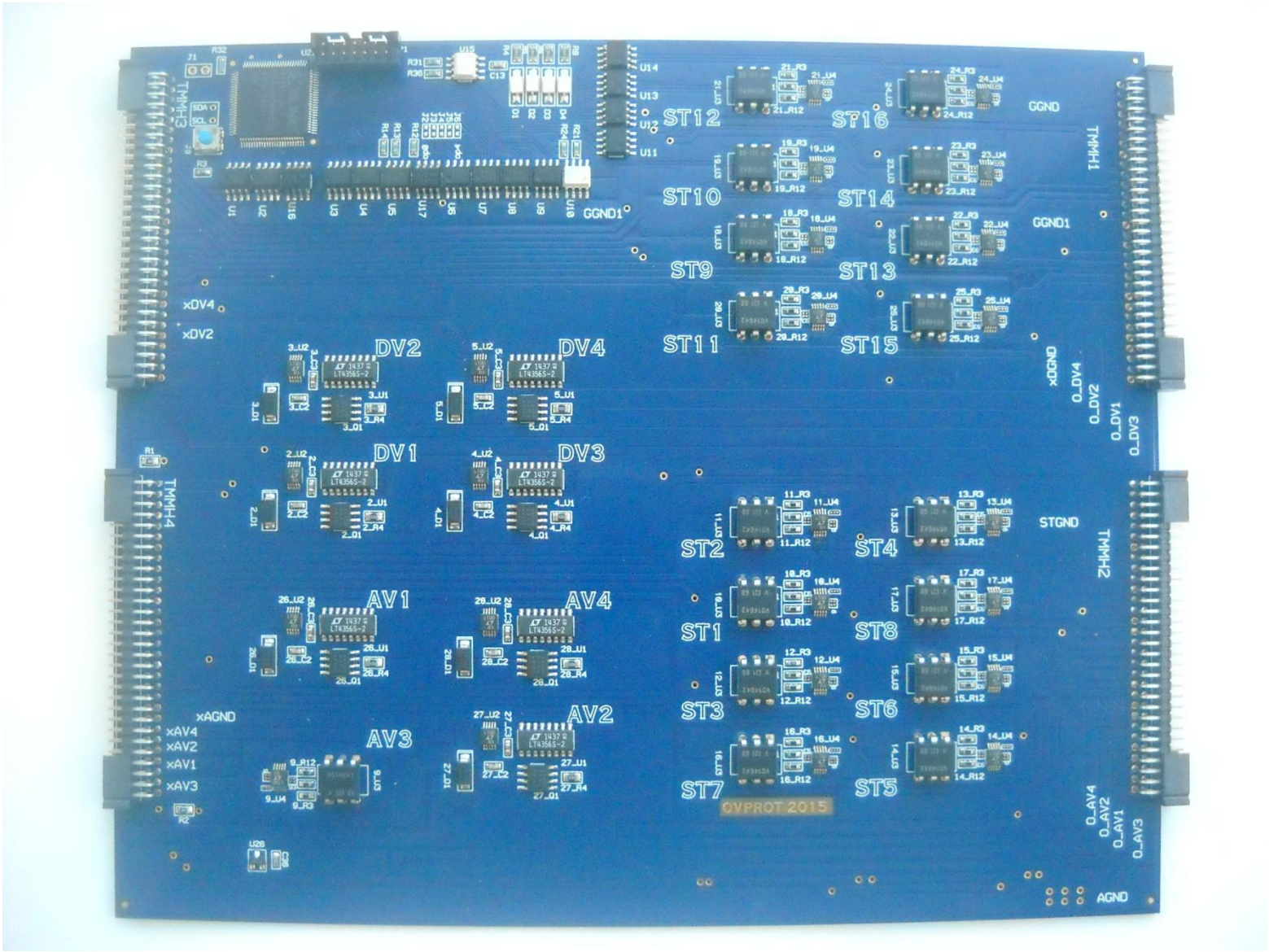
To prevent damage to the PXD detector a separate hardware safety system is implemented.
It contains several interlocks:
- cooling system interlock
- interlock from the Slow Control System
- bad power up/down sequence
- radiation
- Over- voltage interlock – separate module (OVP)

PRODUKCJA

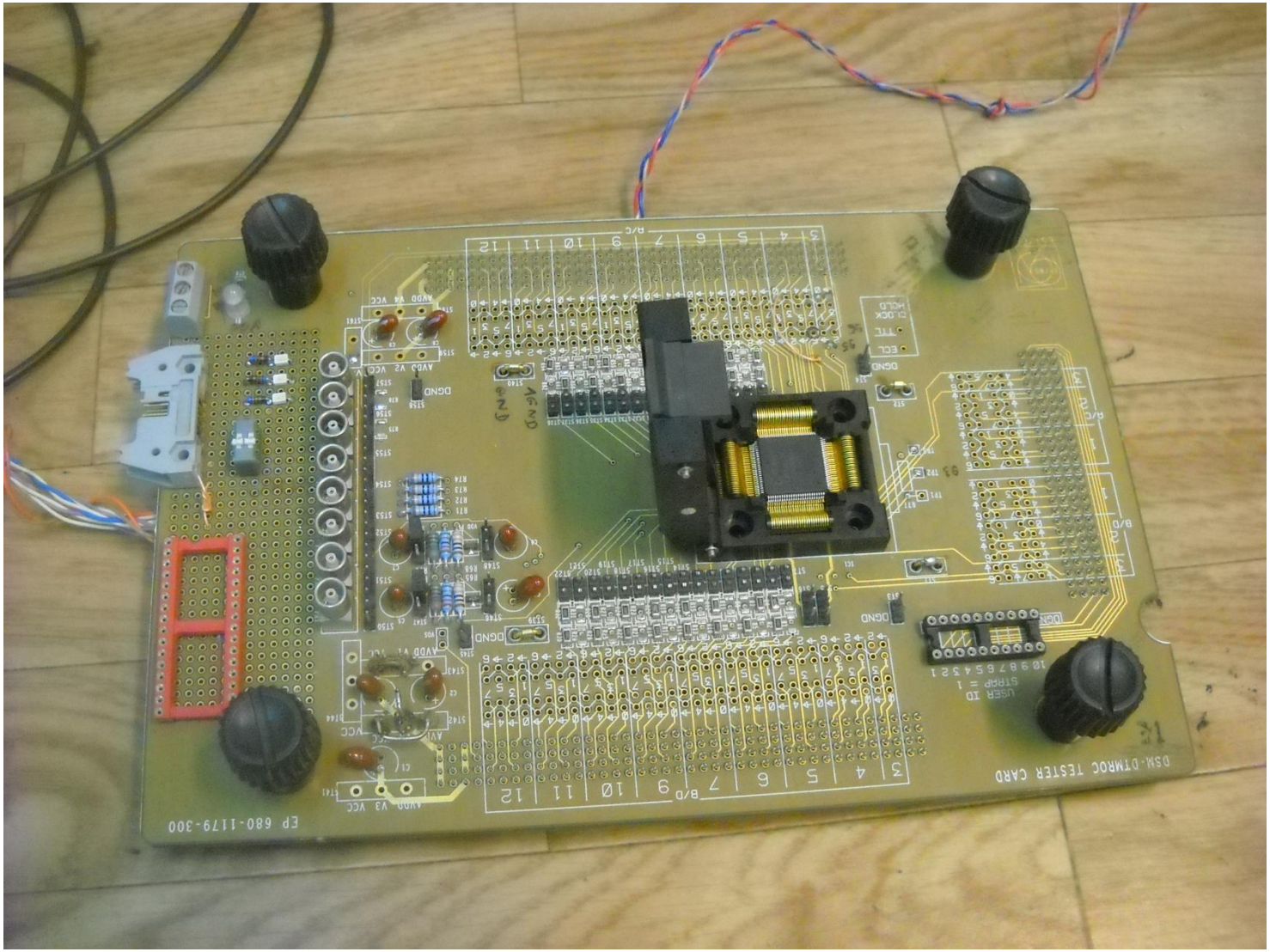
1. Zakup elementów – sprawdzeni dystrybutorzy nie uczestniczą w przetargach
2. Produkcja płytek drukowanych
3. Montaż



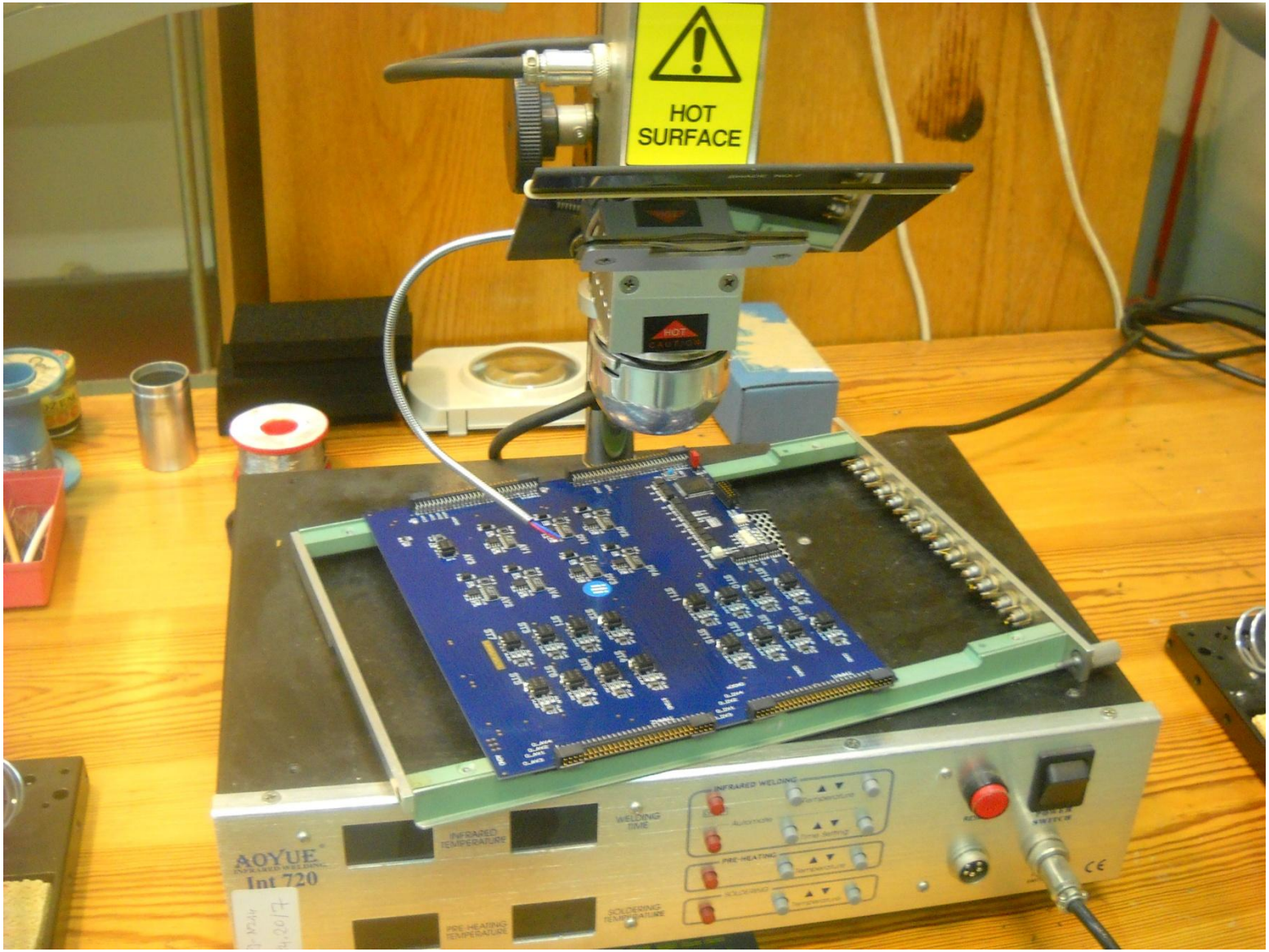
Moduły OVP


DV2
DV4
DV1
DV3
AV1
AV4
AV3
AV2
ST12
ST16
ST10
ST14
ST9
ST13
ST11
ST15
ST2
ST4
ST1
ST8
ST3
ST6
ST7
ST5
GGND
GGND1
STGND
AGND
xDV4
xDV2
xAGND
xAV4
xAV2
xAV1
xAV3
TMHH1
TMHH2
TMHH3
TMHH4
OVPROT 2015

Moduł OVP

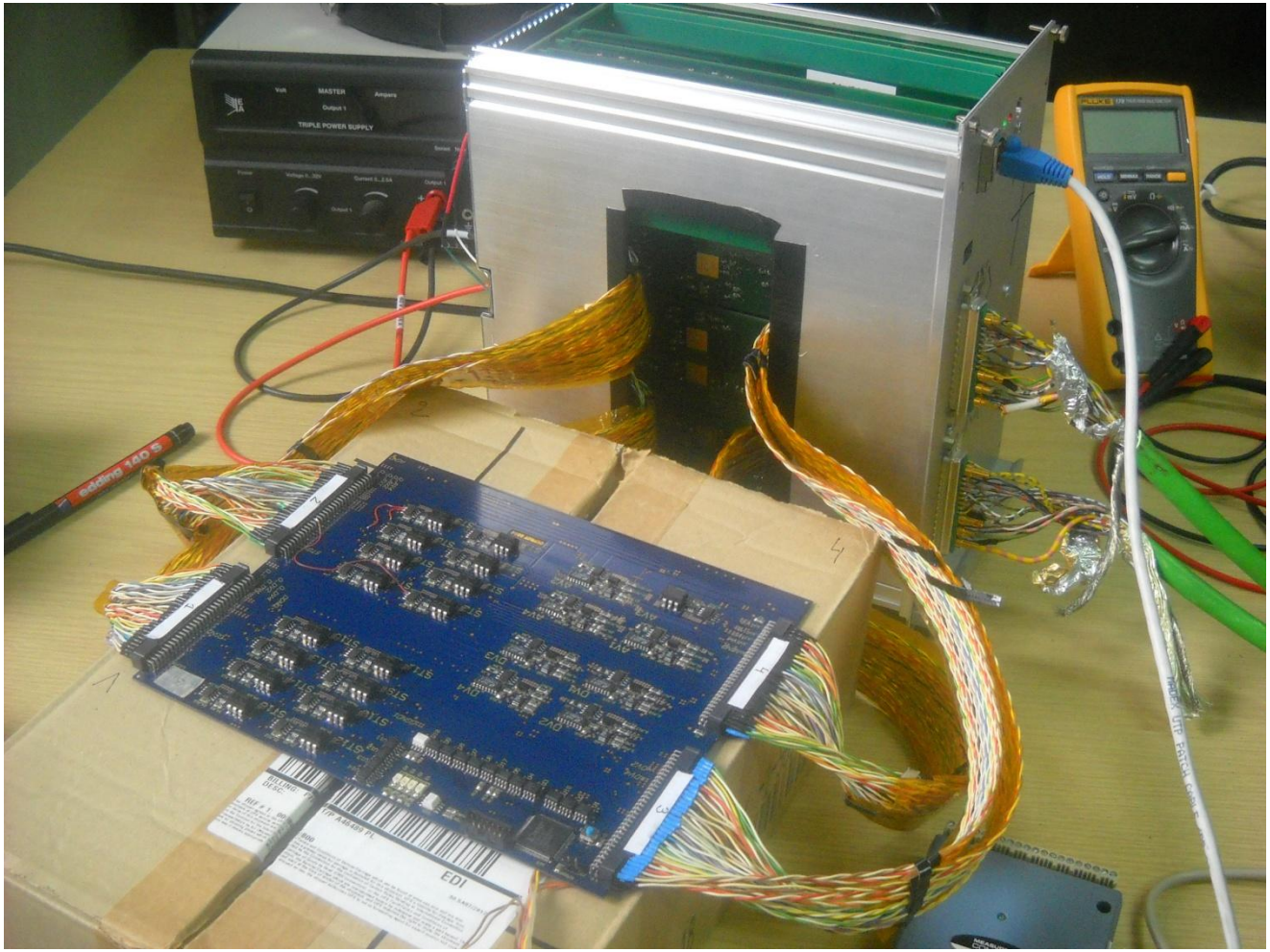


Stanowisko do testowania układów Xilinx.

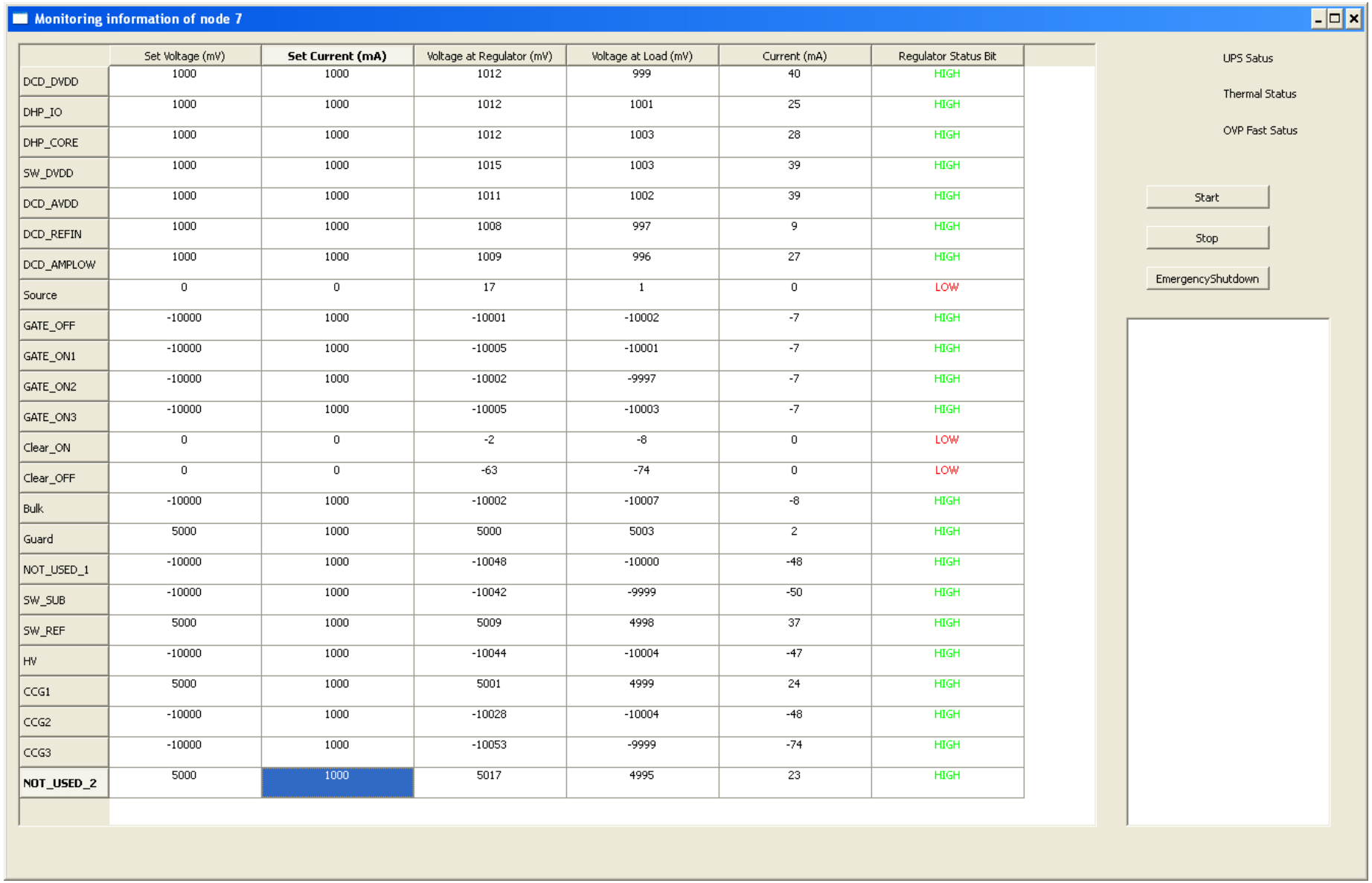


Stacja lutownicza na podczerwień.

Testy

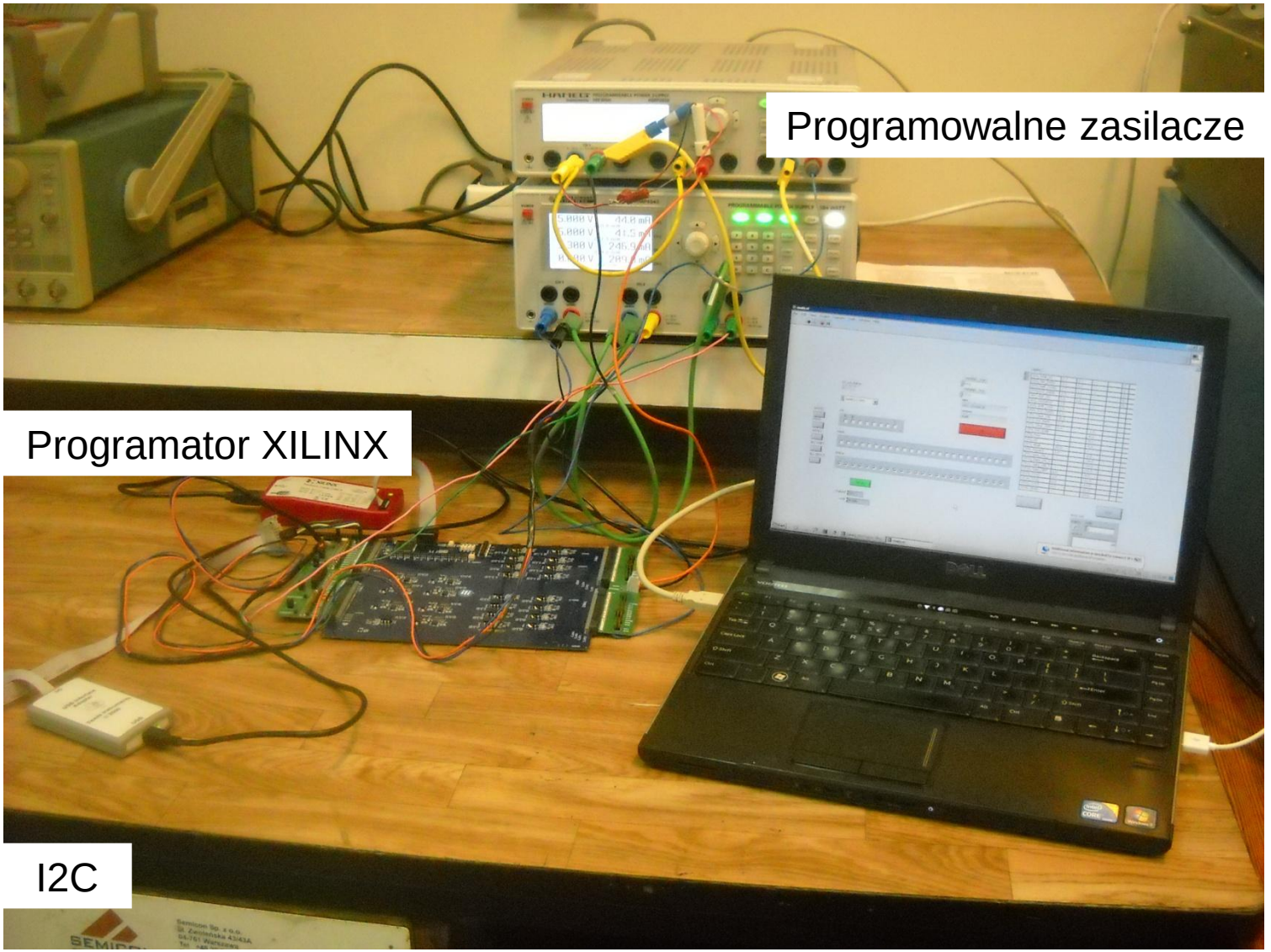


Stanowisko testowe 1



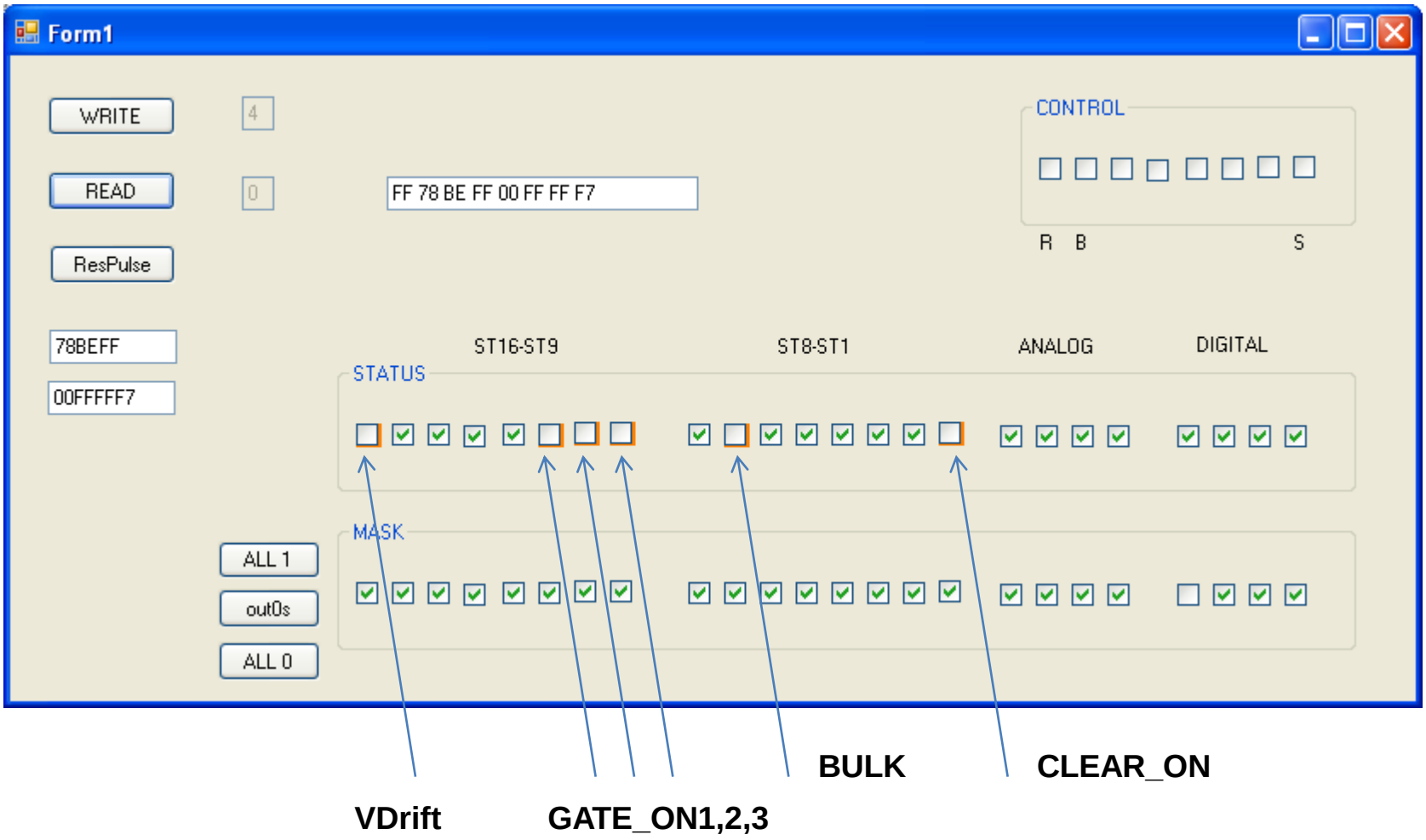
	Set Voltage (mV)	Set Current (mA)	Voltage at Regulator (mV)	Voltage at Load (mV)	Current (mA)	Regulator Status Bit
DCD_DVDD	1000	1000	1012	999	40	HIGH
DHP_IO	1000	1000	1012	1001	25	HIGH
DHP_CORE	1000	1000	1012	1003	28	HIGH
SW_DVDD	1000	1000	1015	1003	39	HIGH
DCD_AVDD	1000	1000	1011	1002	39	HIGH
DCD_REFIN	1000	1000	1008	997	9	HIGH
DCD_AMPLOW	1000	1000	1009	996	27	HIGH
Source	0	0	17	1	0	LOW
GATE_OFF	-10000	1000	-10001	-10002	-7	HIGH
GATE_ON1	-10000	1000	-10005	-10001	-7	HIGH
GATE_ON2	-10000	1000	-10002	-9997	-7	HIGH
GATE_ON3	-10000	1000	-10005	-10003	-7	HIGH
Clear_ON	0	0	-2	-8	0	LOW
Clear_OFF	0	0	-63	-74	0	LOW
Bulk	-10000	1000	-10002	-10007	-8	HIGH
Guard	5000	1000	5000	5003	2	HIGH
NOT_USED_1	-10000	1000	-10048	-10000	-48	HIGH
SW_SUB	-10000	1000	-10042	-9999	-50	HIGH
SW_REF	5000	1000	5009	4998	37	HIGH
HV	-10000	1000	-10044	-10004	-47	HIGH
CCG1	5000	1000	5001	4999	24	HIGH
CCG2	-10000	1000	-10028	-10004	-48	HIGH
CCG3	-10000	1000	-10053	-9999	-74	HIGH
NOT_USED_2	5000	1000	5017	4995	23	HIGH

Displej (ang.dislay) programu monitorującego zasilacz PXD.



Stanowisko testowe 2 do uruchomiania modułów OVP

I2C interface



Displej (ang.display) programu monitorującego moduł OVP.

Raporty

Belle II Weekly Report (Summary) September 9th 2017

Services and PS (Stefan Rummel):

Tests at Bonn showed that the GCK distortion problem when transmitted over the camera link cable is solved when a "pre-emphasis" circuit is introduced at the DHE side. This patch will be used for the phase 2 setup as a small PCB external of the DHE. For the final system, the circuit has to be implemented in the interface cards of the DHH system.

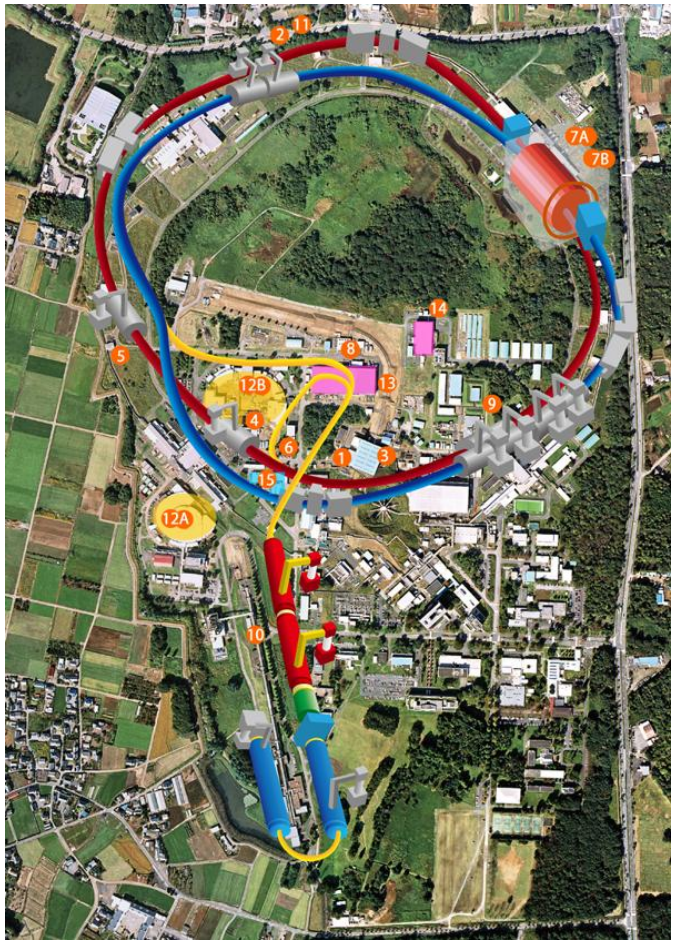
Power Supplies:
The over voltage protection boards (OVP) are now available at LMU Munich and will be incorporated into the phase3 power supplies. The phase2 power supplies (already on their way to KEK) will also get the OVP boards as well as all PS systems used in the different test setups.
Please note, if the assumption that first three ladders were damaged due to a PS failure is right, the OVP card would have prevented that.

Fragment raportu z dnia 9 września 2017

Belle II Weekly Report (Summary) September 16th 2017

Ladder assembly (Hans-Guenther Moser): As previously reported three ladders showed electrical shorts after the ladder gluing. Optical inspections and electrical measurements provided no indication that this is due to mechanical damage during the gluing procedure. We had the suspicion that the damage was caused by the test setup used after the gluing. This was motivated by the fact that only the backward module on the ladder showed the damage, not the forward part. As cross check a ladder was reversed and the forward module measured with the backward setup. Indeed we observed a short in the forward module which had passed all tests before. This is a strong evidence that the setup causes the damage probably by providing wrong voltages. However, when we tried to reproduce this the next day, the short was gone. Not only that the module cured itself, while the other shorts seen before persisted, the setup also looks ok now. It seems that the damage needs some time to ‘ burn in’ and the setup has been fixed while we dis- and re-assembled it during the tests. **Investigations continue and the power supplies will be equipped with an overvoltage protection which will avoid possible damage in future.**

Fragment raportu z dnia 16 września 2017

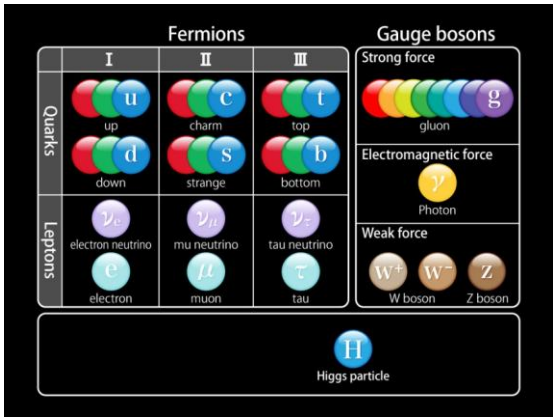




Makoto Kobayashi



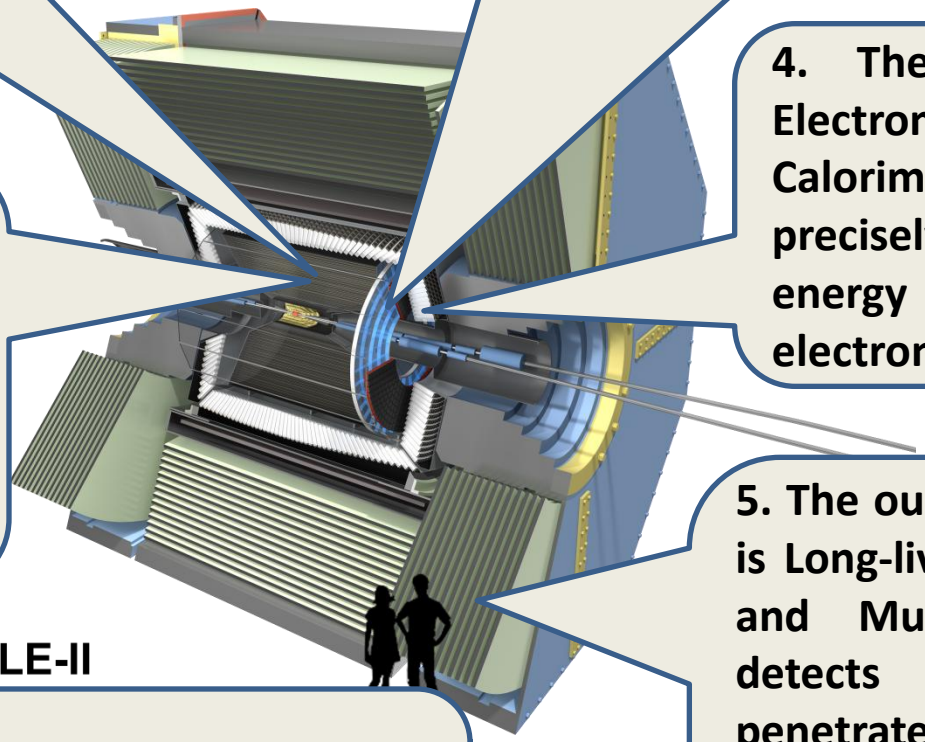
Toshihide Maskawa



The Belle II experiment is being constructed at SuperKEKB asymetric electron-positron collider in Tsukuba, Japan. It is focused on flavor physics and CP violation studies in B meson decays. In 2001 it's predecessor, the Belle experiment, successfully measured CP violation as predicted by Koayashi-Maskawa theory. They won the Nobel Prizes in Physics in 2008.

2. Particles then pass through the Central Drift Chamber. Here they ionize the gas wich fills the detector. In this way a particle's trajectory and momentum is obtained.

3. Next comes the TOP counter and Aerogel RICH Counter. A charged particle emits Cherenkov radiation when it enters these detectors. The timing and pattern information of detected Cherenkov radiation tells us what kind of particle it is.



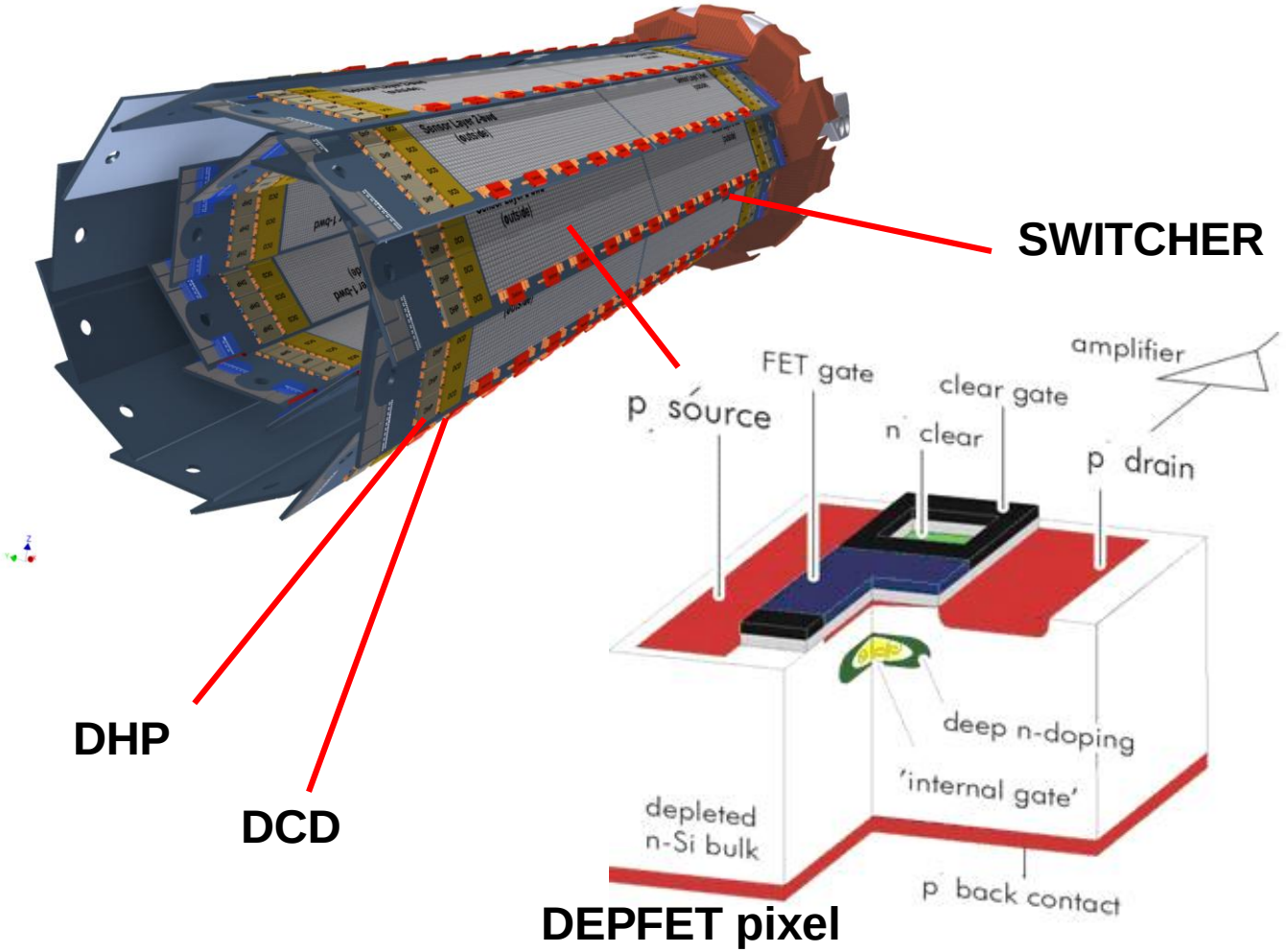
4. Then there is an Electromagnetic Calorimeter. This detector precisely measures the energy of photons and electrons.

1. The Pixel Detector and Silicon Vertex detector are located closest to the interaction point. They precisely detect the path of charge particle.

BELLE-II

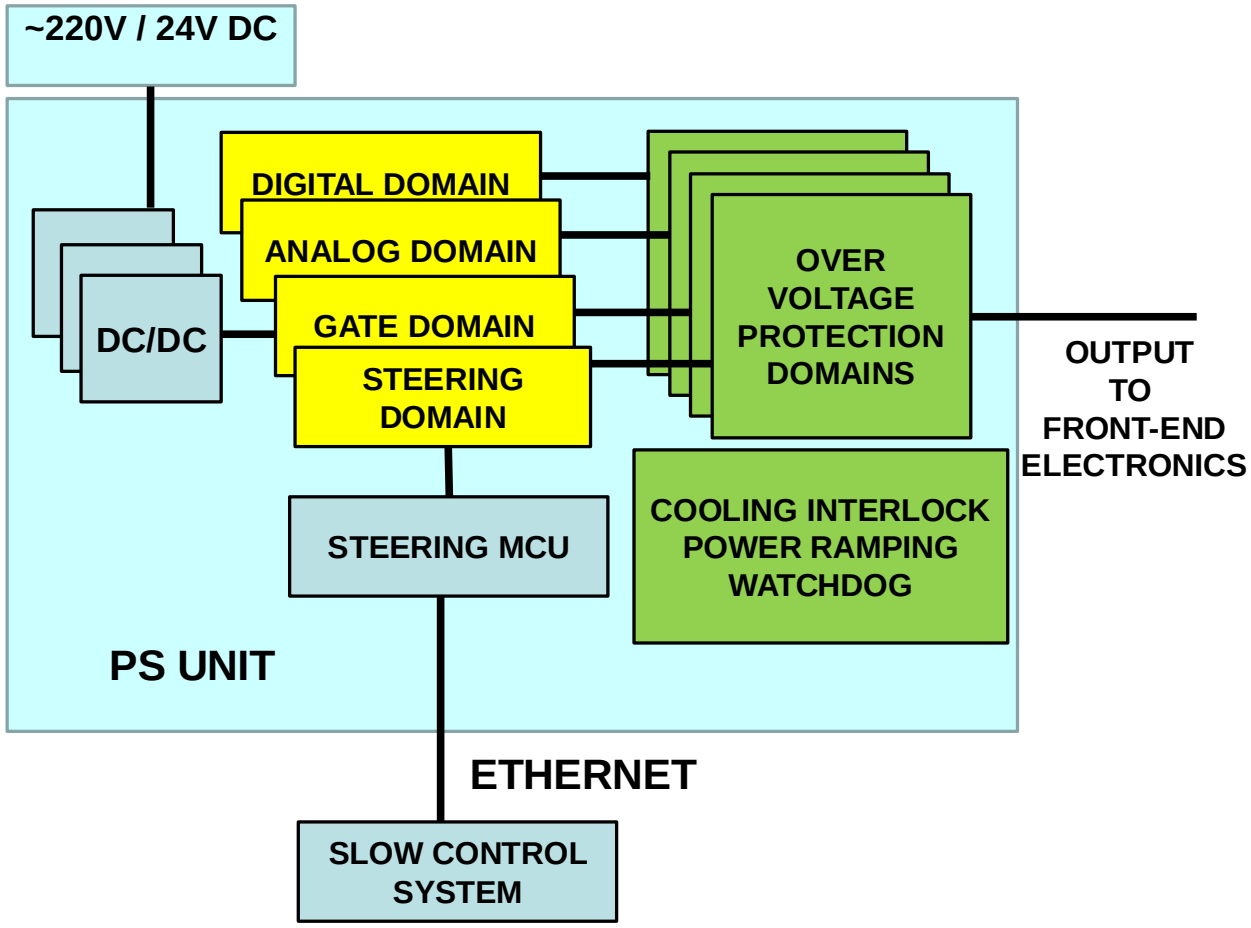
5. The outer-most detector is Long-living neutral Kaon and Muon detector. It detects muons, which penetrate most of the detector and neutral Kaons, which can not be measured with the inner detectors.

6. With these seven kinds of detectors we can tell what is really happening at the point of electron-positron collision.
https://www.youtube.com/user/KEKphysics



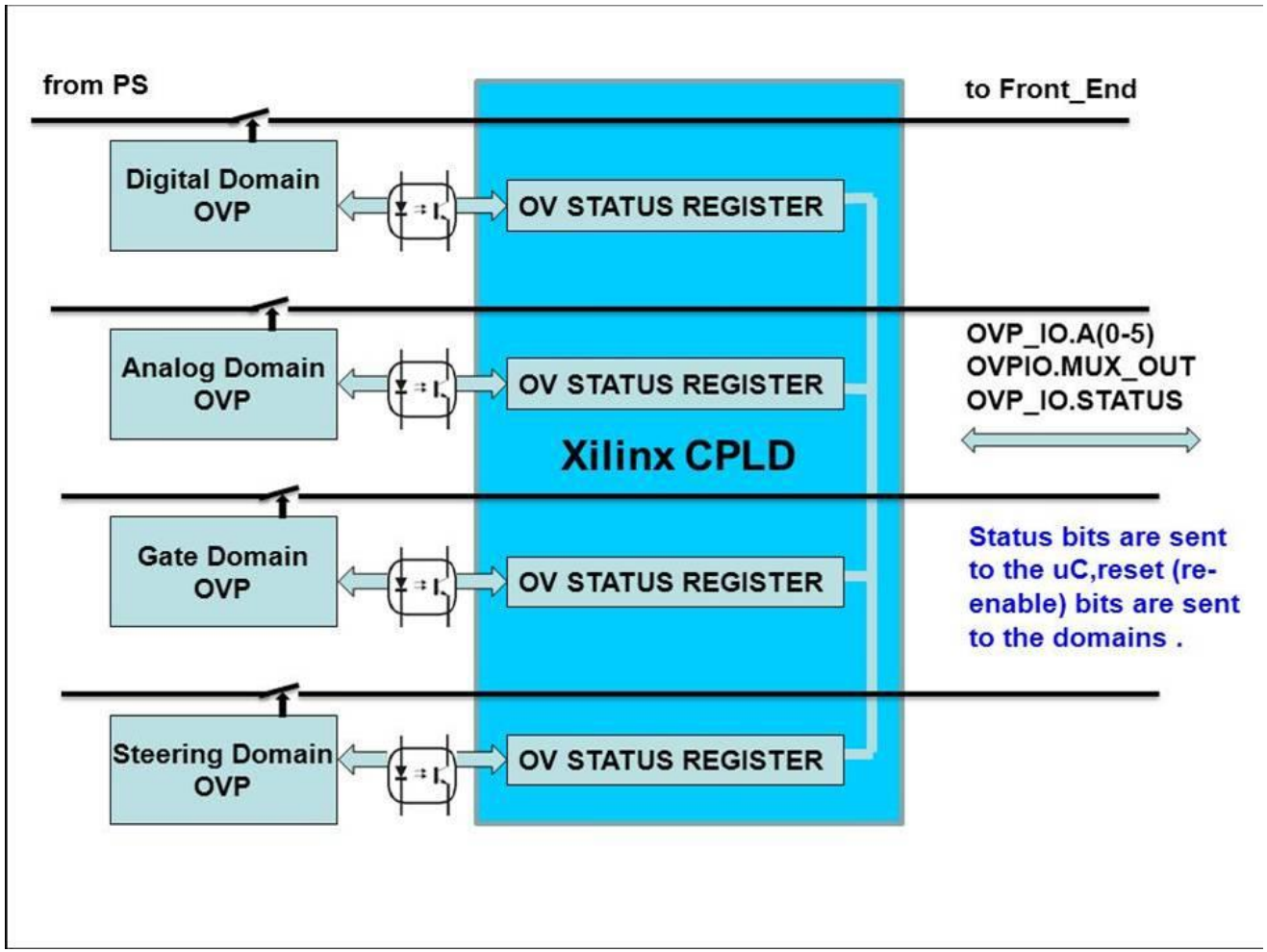
DEPFET pixel

View of the silicon pixel detector PXD and one DEPFET pixel, fully depleted silicon substrate with p-channel MOSFET as active sensor. There are 40 modules of arrays of DEPFET pixels in two layers. Inner part has 8 and outer part 12 modules each with 250 times 768 pixels. All PXD has 7680000 pixels. The "Drain Current Digitizers" (DCD), which digitize the MOSFET currents from a row of pixels, the "Digital Handling Processor" (DHP), which does the zero-suppression of the "empty" pixels; and the "SWITCHERs," which switch on a pixel row to send the currents to the DCD.



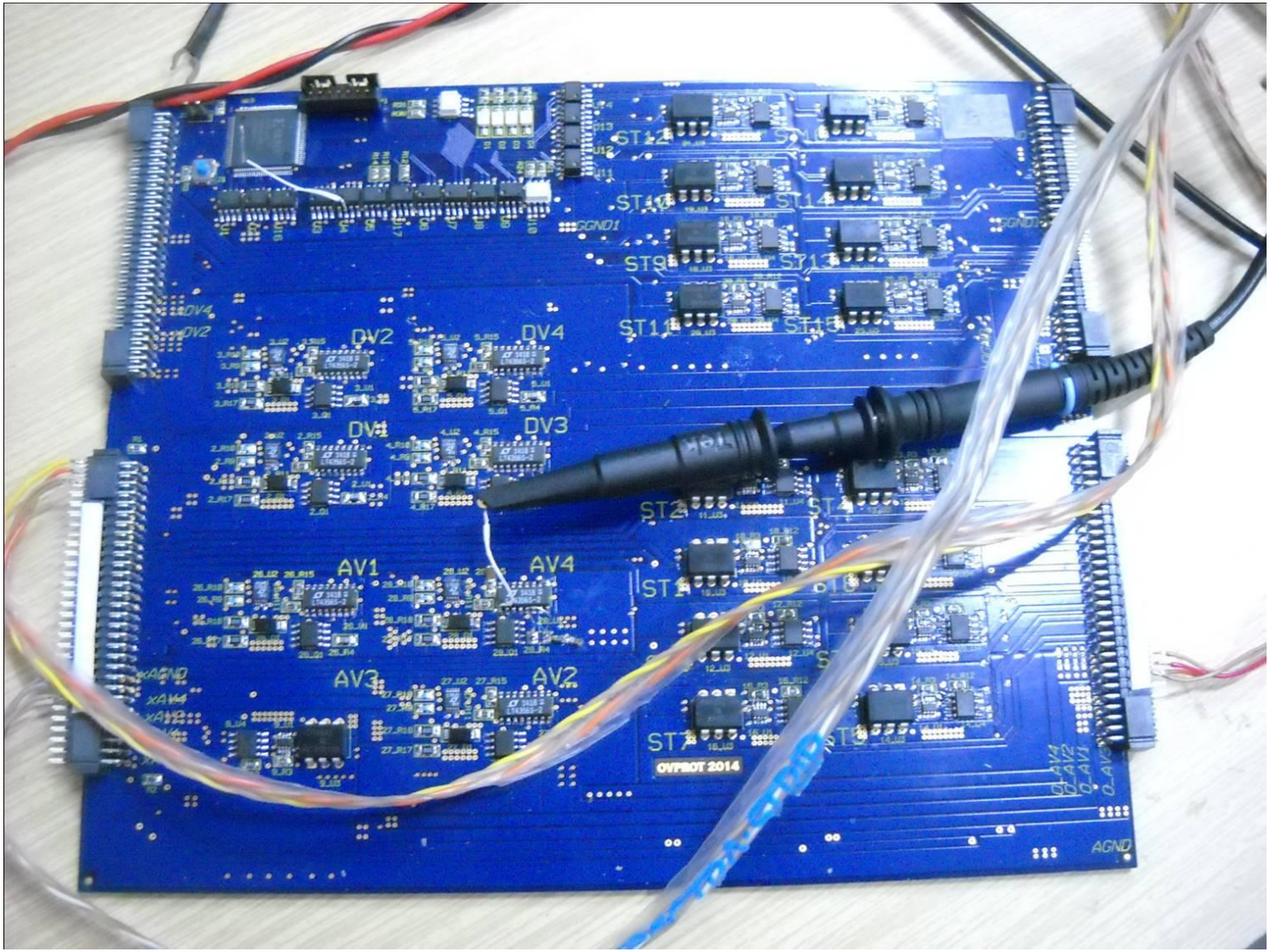
Block diagram of a single PS module of the power supply system of the PXD detector.

Voltage regulators are placed on grounds isolated domains (yellow) and power supplies lines pass through the Over Protection Module to outputs placed in the middle of the Belle II. Green parts show elements of the Safety System.

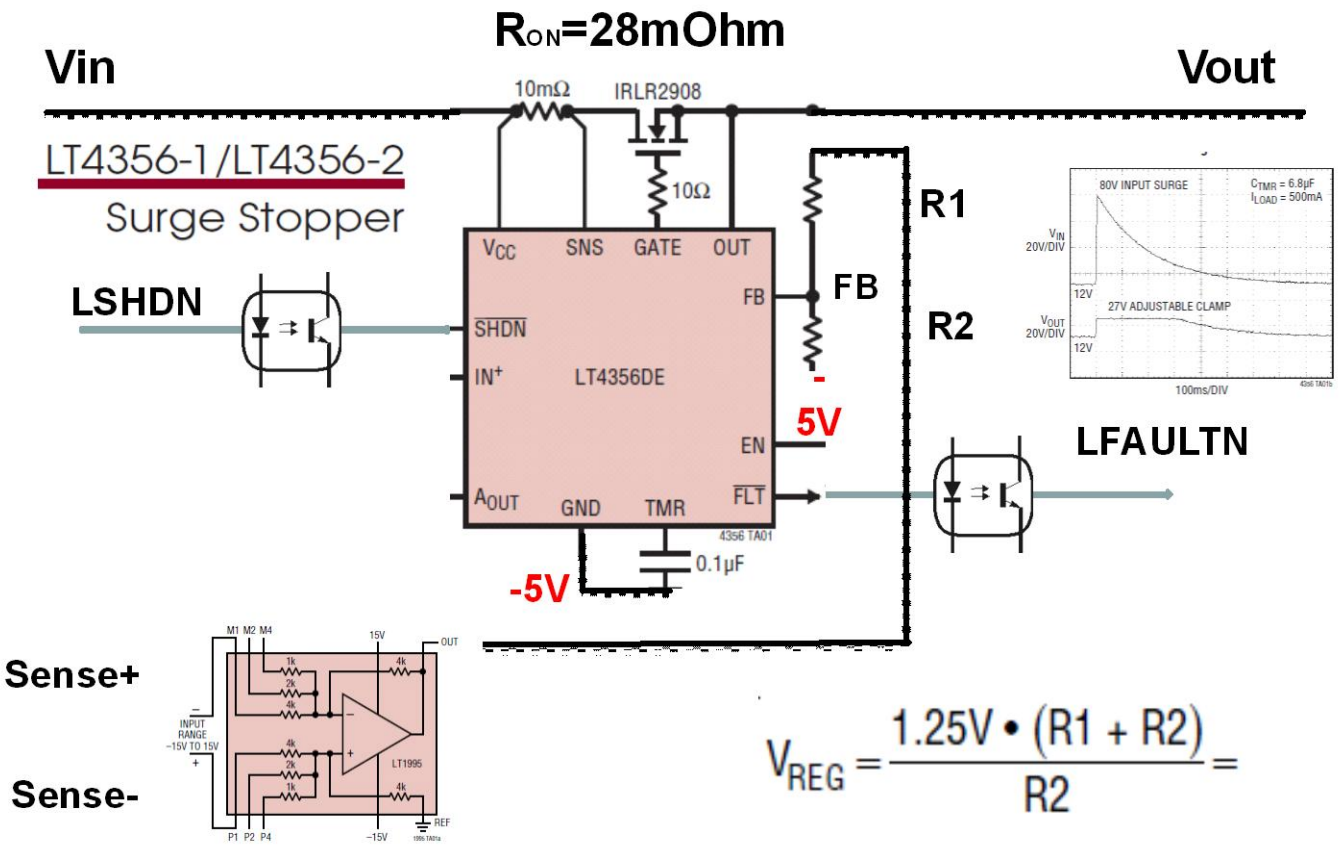


Block diagram of the Over Voltage Protection module.

The OVP module protects 22 voltages supplying front-end electronics situated ~ 15 m outside of the Belle II experiment.



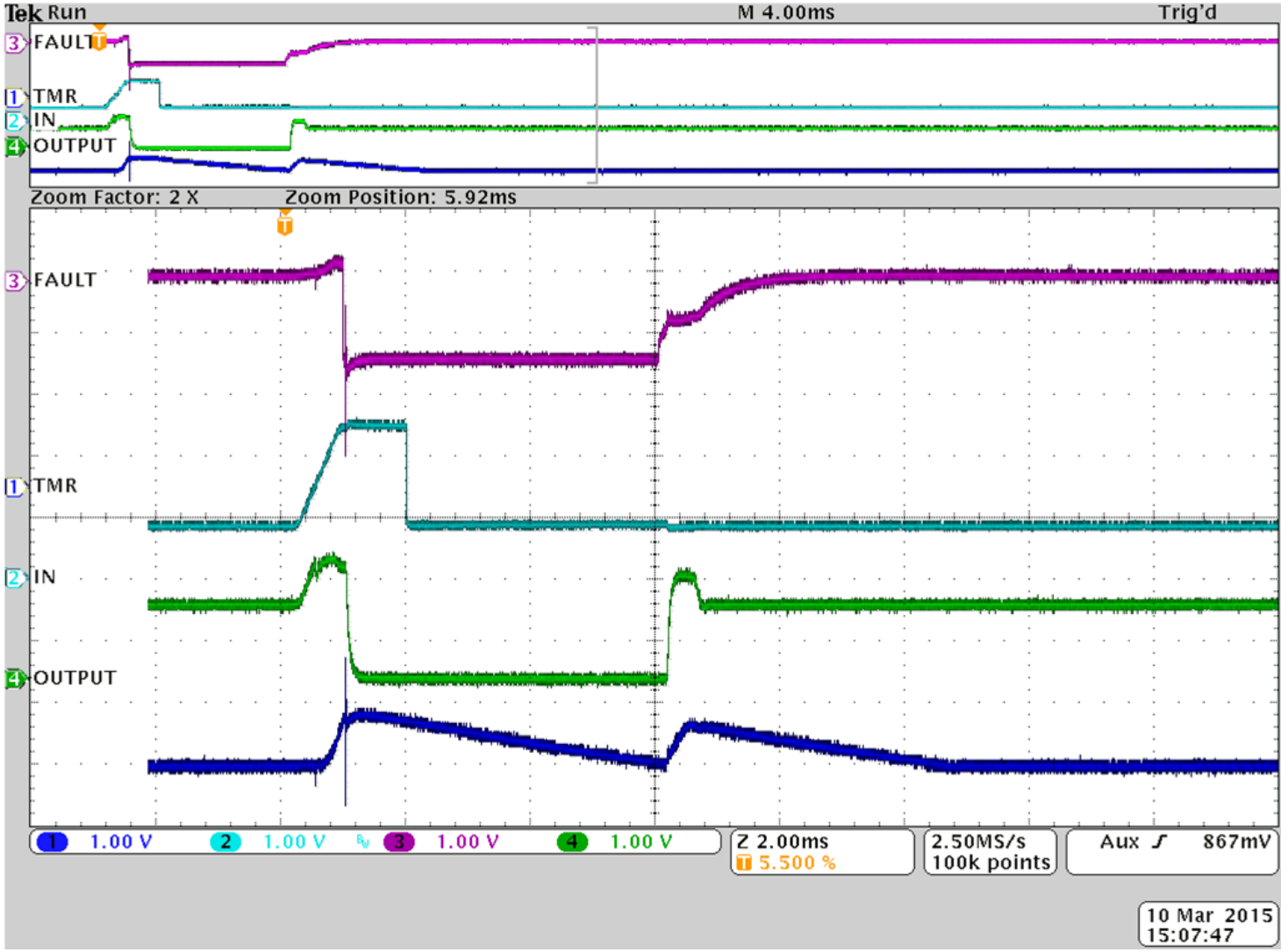
View of the Over Protection Module.



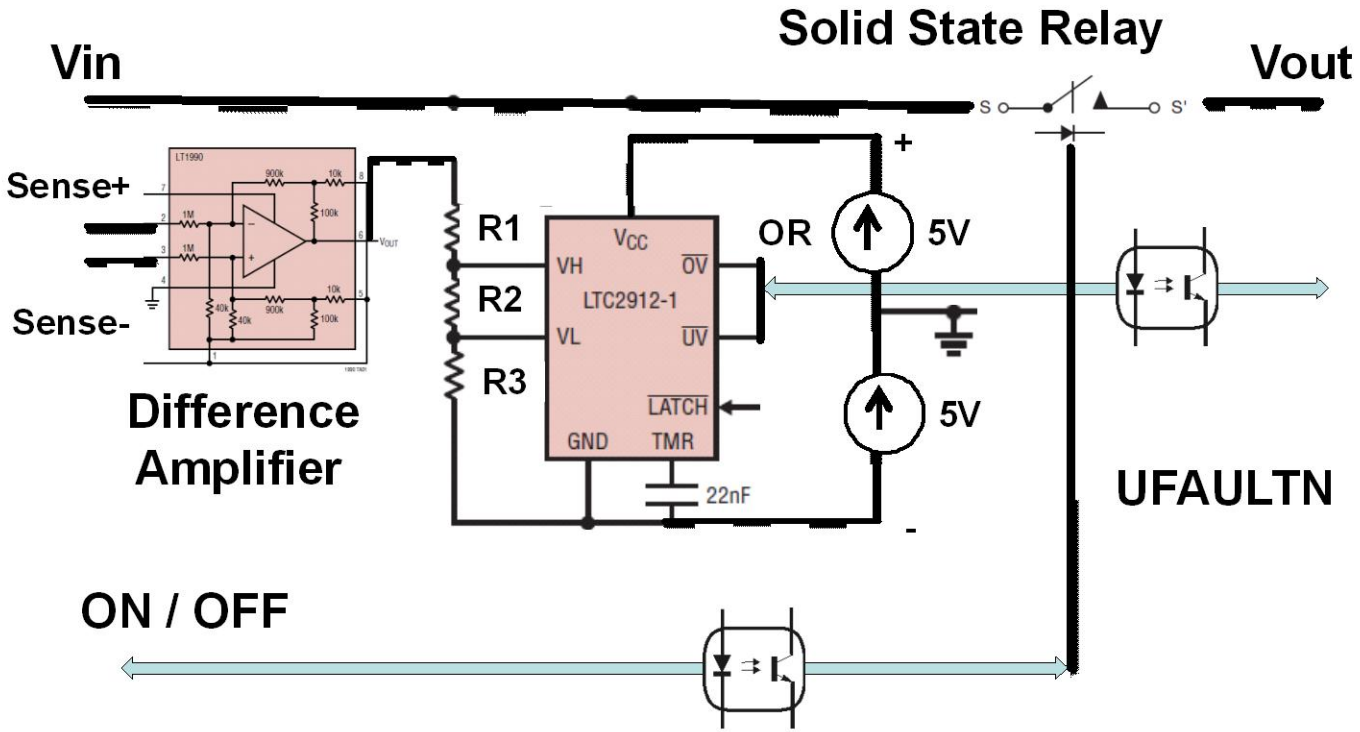
Gain Selectable Amplifier

A simplified schematic of the LT4356 [6] protection of the Analog and Digital domains.

A difference amplifier converts the differential voltage on the sense wires to the single-ended, connected to the Feedback Input (FB). The FB voltage value greater than 1.25V results in lowering the potential of the NMOS gate and limiting the supply current and voltage.



View from oscilloscope: LT4356 protector regulates output voltage from PS during transient (light blue). If transient persists output voltage is switched off (green) and FAULT state (purple) is generated. Capacitor connected to TMR pin (blue) sets the time for early warning, fault and cool down periods.



The Gate and Steering domains exploit a voltage monitor LTC2912 [6] driving a Solid State Relay. After detecting an „out of the window" error condition the channel and a whole domain is switched off.

This project is a piece of hardware contribution of Krakow (Polish) group to the Belle II experiment.

The former Belle experiment produced many results that support the Standard Model. Nevertheless the Standard Model does not answer many important questions and physicist believe that there should be „New Physics” beyond it. This is the main motivation to build new, better accelerator (SuperKEKB) and spectrometer (Belle II) equipped with new detectors.
One of such a detector is pixel detector PXD based on the DEPFET technology invented at the Max-Planck-Institute for Physics and produced in the Semiconductor Laboratory of the Max-Planck Society in Munchen.

An essential part of the PXD detector is power supply system which is quite complex.
In total 22 voltages must be supplied to each detector module.
Hardware failures in the power supply or bad commands from the slow control system could lead to higher than intended voltages being sent to the detector.
To provide protection for the detector and front-end electronic, overvoltage protection (OVP) circuits are placed in all power supply outputs.

Here is shown one detector module with Power Supply equipped with overvoltage protection module (OVP).